

What is claimed is:

1 1. A dynamic random access memory cell layout,
2 comprising:

3 a first gate conductor pair and a second gate conductor
4 pair extending along a first direction, in which
5 each gate conductor pair comprises a first gate
6 conductive line and a second gate conductive
7 line;

8 a bitline pair extending along a second direction and
9 intersecting the gate conductor pairs, in which
10 the bitline pair comprises a first bitline and a
11 second bitline;

12 a first active area extending along the second
13 direction, crossing the first gate conductor pair
14 and corresponding to the first bitline; and

15 a second active area extending along the second
16 direction, crossing the second gate conductor
17 pair and corresponding to the second bitline;

18 wherein, each active area comprises:

19 a first deep trench and a second deep trench formed in
20 a substrate underneath the first gate conductive
21 line and the second gate conductive line,
22 respectively;

23 a bitline contact formed between the first gate
24 conductive line and the second gate conductive
25 line, in which the bitline contact is
26 electrically connected to the corresponding
27 bitline;

28 a common source/drain region formed in the substrate
29 between the first gate conductive line and the
30 second gate conductive line, in which the common
31 source/drain region is electrically connected to
32 the bitline contact;
33 a first vertical transistor formed overlying the first
34 deep trench, in which the first vertical
35 transistor comprises a first buried strap out-
36 diffusion region formed in the substrate adjacent
37 to one sidewall of the first deep trench; and
38 a second vertical transistor formed overlying the
39 second deep trench, in which the second vertical
40 transistor comprises a second buried strap out-
41 diffusion region formed in the substrate adjacent
42 to one sidewall of the second deep trench.

1 2. The dynamic random access memory cell layout as
2 claimed in claim 1, wherein the first deep trench is
3 partially overlapped with the first vertical transistor, and
4 the sidewall profile of the first deep trench on the
5 overlapping portion is a line shape.

1 3. The dynamic random access memory cell layout as
2 claimed in claim 1, wherein the second deep trench is
3 partially overlapped with the second vertical transistor,
4 and the sidewall profile of the second deep trench on the
5 overlapping portion is a line shape.

1 4. The dynamic random access memory cell layout as
2 claimed in claim 1, wherein the first deep trench is
3 partially overlapped with the first vertical transistor, and

4 the sidewall profile of the first deep trench on the
5 overlapping portion comprises at least three edges.

1 5. The dynamic random access memory cell layout as
2 claimed in claim 4, wherein the sidewall of the first deep
3 trench on the overlapping portion is a \sqcup -shaped profile.

1 6. The dynamic random access memory cell layout as
2 claimed in claim 1, wherein the second deep trench is
3 partially overlapped with the second vertical transistor,
4 and the sidewall profile of the second deep trench on the
5 overlapping portion comprises at least three edges.

1 7. The dynamic random access memory cell layout as
2 claimed in claim 6, wherein the sidewall of the second deep
3 trench on the overlapping portion is a \sqcup -shaped profile.

1 8. The dynamic random access memory cell layout as
2 claimed in claim 1, further comprising a first deep trench
3 capacitor formed at the lower portion of the first deep
4 trench.

1 9. The dynamic random access memory cell layout as
2 claimed in claim 1, further comprising a second deep trench
3 capacitor formed at the lower portion of the second deep
4 trench.

1 10. A fabrication method for a dynamic random access
2 memory cell layout, comprising the steps of:

3 providing a semiconductor silicon substrate having an
4 array area and a support area;

5 forming a pad layer overlying the semiconductor silicon
6 substrate, in which the pad layer comprises a
7 predetermined deep trench pattern;
8 forming a first deep trench and a second deep trench in
9 the semiconductor silicon substrate within the
10 array area;
11 forming a first deep trench capacitor and a second deep
12 trench capacitor at the lower portions of the
13 first deep trench and the second deep trench,
14 respectively;
15 forming a collar dielectric layer on the sidewalls of
16 the first deep trench and the second deep trench,
17 respectively, in which the collar dielectric
18 layer is disposed over the first deep trench
19 capacitor and the second deep trench capacitor;
20 forming a polysilicon layer in the first deep trench
21 and the second deep trench, in which the
22 polysilicon layer is surrounded by the collar
23 dielectric layer;
24 forming a first buried strap out-diffusion region and a
25 second buried strap out-diffusion region in the
26 semiconductor silicon substrate adjacent to the
27 sidewalls of the first deep trench and the second
28 deep trench, respectively, in which the first
29 buried strap out-diffusion region and the second
30 buried strap out-diffusion region are adjacent to
31 the polysilicon layer in the first deep trench
32 and the second deep trench, respectively;

33 forming a top isolating layer to cover the top of the
34 polysilicon layer in the first deep trench and
35 the second deep trench;
36 forming two first shallow trenches in the semiconductor
37 silicon substrate within the array area to
38 separate the active area from other areas, in
39 which the first shallow trenches are outside the
40 first deep trench and the second deep trench is
41 within the array area;
42 forming a second shallow trench in the semiconductor
43 silicon substrate within the support area;
44 forming a liner on the substrate;
45 forming a first isolating layer in the first shallow
46 trenches and the second shallow trench, in which
47 the top of the first isolating layer is leveled
48 off with the top of the liner;
49 forming a photoresist layer to cover the support area;
50 removing the first isolating layer formed in the first
51 shallow trenches within the array area;
52 removing the photoresist layer, the exposed liner and
53 the pad layer, in which the semiconductor silicon
54 substrate within the active area of the array
55 area protrude from the top isolating layer;
56 forming a gate oxide layer on the exposed surface of
57 the semiconductor silicon substrate;
58 forming a gate conductive structure on the active area
59 between the first deep trench and the second deep
60 trench;
61 forming a second isolating layer to fill the first
62 shallow trenches, in which the top of the second

63 isolating layer is leveled with the top of the
64 gate conductive structure; and
65 forming a first contact hole penetrating the gate
66 conductive structure and the gate oxide layer to
67 expose the semiconductor silicon substrate.

1 11. The fabrication method for a dynamic random access
2 memory cell layout as claimed in claim 10, further
3 comprising the steps of:

4 forming a spacer on the sidewall of the first contact
5 hole;

6 forming a common source/drain diffusion region in the
7 semiconductor substrate exposed within the first
8 contact hole;

9 forming a first inter-layered dielectric and a second
10 inter-layered dielectric overlying the
11 semiconductor silicon substrate;

12 forming a second contact hole which penetrates the
13 second inter-layered dielectric and the first
14 inter-layered dielectric to expose the first
15 contact hole and the common source/drain
16 diffusion region;

17 forming a contact layer in the second contact hole; and

18 forming a bitline overlying the second inter-layered
19 dielectric, in which the bitline is electrically
20 connected to the contact layer.

1 12. The fabrication method for a dynamic random access
2 memory cell layout as claimed in claim 10, wherein the liner
3 is a silicon nitride layer.

Client's ref. :91234
Our ref: 0548-10164-us/final/Cherry/Steve

1 13. The fabrication method for a dynamic random access
2 memory cell layout as claimed in claim 10, wherein the first
3 isolating layer is a HDP (high-density plasma) oxide layer.

1 14. The fabrication method for a dynamic random access
2 memory cell layout as claimed in claim 10, wherein the gate
3 conductive structure comprises a polysilicon layer, a
4 metallic silicide layer and a nitride cap layer.

1 15. The fabrication method for a dynamic random access
2 memory cell layout as claimed in claim 10, wherein the
3 second isolating layer is a HDP (high-density plasma) oxide
4 layer.

1 16. The fabrication method for a dynamic random access
2 memory cell layout as claimed in claim 11, wherein the
3 spacer is a silicon nitride layer.

1 17. The fabrication method for a dynamic random access
2 memory cell layout as claimed in claim 11, wherein the first
3 inter-layered dielectric is a BPSG layer.

1 18. The fabrication method for a dynamic random access
2 memory cell layout as claimed in claim 11, wherein the
3 second inter-layered dielectric is a TEOS oxide layer.